

**Claims**

What is claimed is:

- 1 1. A digital signal processor comprising:
  - 2 an analog front end including an analog-to-digital converter for
  - 3 receiving an input signal;
  - 4 a digital base-band processor having a latency period for detecting a
  - 5 signal, coupled to the analog front end;
  - 6 a shift register for tracking data representing the relative amplitude of
  - 7 samples of the input signal;
  - 8 a gain control counter controlled by a current relative amplitude of
  - 9 sample of the input signal and an output from the shift register, coupled to
  - 10 the shift register; and
- 11 a gain control circuit coupled to the counter for controlling gain of the
- 12 input signal.

- 1 2. The digital signal processor of claim 1 wherein the shift register tracks
- 2 data representing a period equal to at least the latency period.

- 1 3. The digital signal processor of claim 2 wherein the gain control
- 2 counter ceases to be controlled by the output of the shift register once the

3 base-band detector detects a signal of a predetermined threshold from the  
4 analog front end.

1 4. The digital signal processor of claim 2 wherein the gain control circuit  
2 includes a comparator for comparing a count in the gain control counter with  
3 a predetermined count and based upon the results of the comparison,  
4 adjusts the gain of the input signal.

1 5. The digital signal processor of claim 1 wherein the shift register  
2 comprises a first shift register and a second shift register.

1 6. The digital signal processor of claim 5 wherein the first shift register is  
2 coupled to a first comparator which compares samples of the input signal  
3 with a lower threshold level.

1 7. The digital signal processor of claim 6 wherein the second shift  
2 register is coupled to a second comparator which compares samples of the  
3 sampled input signal with an upper threshold level.

1    8.     The digital signal processor of claim 7 wherein the first and second  
2    shift registers each have a number of stages approximately equal to the  
3    number of samples occurring during the latency period.

1    9.     The digital signal processor defined by claim 8 wherein the gain  
2    control counter comprises a first gain control counter and a second gain  
3    control counter, the first gain control counter being controlled by the first  
4    comparator and the first shift register and the second gain control counter  
5    being controlled by the second comparator and the second shift register.

1    10.    The digital signal processor defined by claim 9 wherein the control of  
2    the first and second gain control counter by the first and second shift  
3    registers, respectively, ceases once the band-based processor detects the  
4    signal having the predetermined threshold.

1    11.    The digital signal processor defined by claim 10 including a first logic  
2    circuit coupled to receive a most significant bit from the first shift register and  
3    an output of the first comparator for providing a count-up and count-down  
4    signal to the first gain control counter.

1    12.    The digital signal processor of claim 11 including a second logic circuit  
2    coupled to receive a most significant bit from the second shift register and an  
3    output of the second comparator for providing a count-up and count-down  
4    signal to the second gain control counter.

1    13.    The digital signal processor of claim 10 including a third comparator  
2    for comparing a current count in the first gain control counter with a first  
3    predetermined count and for providing an output for increasing gain if the  
4    current count is less than the first predetermined count.

1    14.    The digital signal processor of claim 11 including a fourth comparator  
2    for comparing the current count in the second gain control counter with a  
3    second predetermined count and for decreasing gain if the current count is  
4    greater than the second predetermined count.

1    15.    In a digital signal processor having a latency period for detecting a  
2    signal, an improvement comprising:  
3        memory means for recording a history of the relative amplitude of  
4    samples of an input to the processor; and

5        gain control means for controlling the gain of the input to the  
6    processor based upon the current amplitude of the input to the processor and  
7    the relative amplitude of prior input samples recorded in the memory means.

1    16.    The digital signal processor of claim 15 wherein the memory means  
2    stores the relative amplitude of samples for a period of at least equal to the  
3    digital base-band processor latency period.

1    17.    The digital signal processor of claim 16 wherein the memory means  
2    comprises a first and a second shift register.

1    18.    The digital signal processor of claim 17 wherein the gain control  
2    means includes a first counter coupled to receive an output of the first shift  
3    register and a second counter coupled to receive an output of the second  
4    shift register.

1    19.    A method for controlling gain in a digital signal processor comprising:  
2        tracking data representing the relative amplitude of an input signal;  
3        and  
4        controlling the gain by considering a current amplitude and a prior  
5        amplitude from the tracked data.

1    20.    The method defined by claim 19 wherein the controlling of the gain  
2    ceases to consider the tracked data once a signal is detected.

1    21.    The method defined by claim 20 wherein the tracking step comprises,  
2    recording first bits representing samples of the input signal that exceed a first  
3    predetermined threshold and second bits representing samples of the input  
4    signal that are less than a second predetermined threshold.

1    22.    The method defined by claim 21 wherein the processor has a signal  
2    detection latency period and the tracked data is for a period at least as long  
3    as the latency period.